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**Thermal standardization on semiconductor packages -
Part 6: Thermal resistance and capacitance model for transient temperature prediction at junction and measurement points**

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FOREWORD

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IEC 63378-6 has been prepared by subcommittee 47D: Semiconductor devices packaging, of IEC Technical Committee 47: Semiconductor devices. It is an International Standard.

The text of this International Standard is based on the following documents:

Draft	Report on voting
47D/991/CDV	47D/998/RVC

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/publications.

A list of all parts in the IEC 63378 series, published under the general title *Thermal standardization on semiconductor packages*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under webstore.iec.ch in the data related to the specific document. At this date, the document will be

– reconfirmed,

– withdrawn, or

– revised.

INTRODUCTION

The IEC 63378-6 series is composed of the following parts:

– IEC 63378-6-1 [1][1,2] defines the model creation method using a datasheet of semiconductor devices.

– IEC 63378-6-2 [3] defines the model creation method using measurement data of semiconductor devices.

The IEC 63378-6 series includes subjects such as the definition of a new thermal compact model for thermal transient analysis of semiconductor packages, model creation methods, accuracy assessment of these models, etc.

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1 Numbers in square brackets refer to the Bibliography.

2 Under preparation. Stage at the time of publication: IEC APUB 63378-6-1:2026.

3 Under development.

1 Scope

This part of IEC 63378 specifies a thermal resistance and capacitance model for semiconductor packages. This model is named the digital transformation using thermal resistance and capacitance (DXRC) model. It predicts transient temperature at junction and measurement points.

This document applies to semiconductor packages such as TO-252, TO-263, and HSOP. It supports single chip packages dissipated heat from single package surface.

2 Normative references

There are no normative references in this document.

Bibliography

[1] IEC 63378-6-1:–[4], *Thermal standardization on semiconductor packages - Part 6-1: Thermal resistance and capacitance model for transient temperature prediction at junction and measurement points - Model creation method using a datasheet of semiconductor device*

[2] JESD51-14:2010, *Transient Dual Interface Test Method for the Measurement of the Thermal Resistance Junction to Case of Semiconductor Devices with Heat Flow Through a Single Path*

[3] IEC 60050-521:2002, *International Electrotechnical Vocabulary (IEV) – Part 521: Semiconductor devices and integrated circuits*

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[4] Under preparation. Stage at the time of publication: IEC APUB 63378-6-1:2026.