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Hardware-in-the-loop simulation test of power system stability control system

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IEC Secretariat
3, rue de Varembé
CH-1211 Geneva 20
Switzerland

Tel.: +41 22 919 02 11
info@iec.ch
www.iec.ch

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CONTENTS

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Hardware-in-the-loop simulation test of power system stability control system

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IEC TS 63537 has been prepared by subcommittee 8C, Network management in interconnected electric power systems, of IEC technical committee 8: System aspects of electrical energy supply. It is a Technical Specification.

The text of this Technical Specification is based on the following documents:

Draft	Report on voting
8C/157/DTS	8C/169A/RVDTS

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this Technical Specification is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/publications.

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– reconfirmed,
– withdrawn, or
– revised.

1 Scope

This Technical Specification (TS) addresses the requirements for hardware-in-the-loop (HIL) simulation test of power system stability control system (see definition in 3.1.2). Its purpose is to provide guidelines encompassing the use of terms and definitions, as well as the objective and general requirements for HIL simulation test. The TS covers the test requirements, test system, test contents, and test quality management.

This TS improves the safe and stable operation of the power system.

2 Normative references

There are no normative references in this document.

Bibliography

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