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The text of this International Standard is based on the following documents:

Draft	Report on voting
47/3015/FDIS	47/3026/RVD

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/publications.

A list of all parts in the IEC 63287 series, published under the general title *Semiconductor devices - Generic semiconductor qualification guidelines*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under webstore.iec.ch in the data related to the specific document. At this date, the document will be

– reconfirmed,

– withdrawn, or

– revised.

INTRODUCTION

When performing qualification tests, semiconductor device vendors prepare a specific reliability test plan upon consultation with semiconductor device users in order to efficiently carry out the reliability test.

This guideline presents examples of methods for preparing test plans to determine appropriate reliability test conditions, based on the level of quality required in the operating environments of various applications of power semiconductor modules. As a target of reliability, grades have been specified for each of the following applications: automotive, industrial and consumer electronics. Based on the number of annual operating hours, use period and other parameters assumed for each grade, this guideline defines verification methods for the wear-out failure, and proposes appropriate reliability tests. This guideline defines the concept of quality assurance from early failure to wear-out failure. It also presents approaches to appropriately ensure the reliability of power semiconductor modules.

The test conditions and the acceleration factor values presented in this guideline are only examples used for setting reliability test conditions to verify a required level of quality.

NOTE Qualification tests are tests performed by power semiconductor device vendors, taking into account the quality required by the users of their products.

1 Scope

This part of IEC 63287 specifies guidelines for a reliability qualification plan for power semiconductor modules to assure reliability targets over the entire product life.

Power semiconductor modules with incorporated control circuits are excluded. Clamped packages that need external pressure for being mounted in a system are excluded, e.g. disc-type pressure pack devices.

This document is not intended for medical, military, aeronautics and astronautics-related applications.

NOTE Throughout the document, the term power semiconductor module refers to multichip semiconductor power modules as defined in 3.3.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

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[1] JEITA EDR-4711A is the expanded version of IEC63287-1 which specifies for power semiconductor.